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Asst. Commissioner for Patents
Washington, DC 20231

OFGS File No. : IR-1773 (2-2498)
Inventor : Mark PAVIER
Title : POWER SEMICONDUCTOR DIE ATTACH PROCESS USING CONDUCTIVE ADHESIVE FILM
Assignee : International Rectifier Corporation

Enclosed herewith please find the following documents in the above-identified application for United States Letters Patent:

X Print EFS Data Sheet
8 Pages of Specification including Abstract and Claims
11 Numbered Claims Calculated as 11 Claims for Fee Purposes
2 Sheets of Drawing Containing Figures 1 to 10. (Informal)
X Declaration and Power of Attorney
X Priority is Claimed under 35 U.S.C. §120:
X Assignment
X Return-Addressed Post Card

OFGS Check No. 3245, which includes the fee of $750.00, calculated as follows:

Basic Filing Fee:	$ 710.00
Additional Filing Fees:	
Total Number of Claims in Excess of 20, times $18:	-
Number of Independent Claims in Excess of 3, times $80: . .	-
One or More Multiple Dependent Claims: Total $270.	-
Total Filing Fees or	$ 710.00
Total Filing Fee Reduced 50% for Small Entity:	-
Assignment Recording Fee: $40	$ 40.00
TOTAL Filing Fee and Assignment Recording Fee:	$ 750.00

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed, or if any additional fee during the prosecution of this case is not paid, the Patent and Trademark Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

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Signature

November 22, 2000
Date of Signature

SHW:KS1:md1

Respectfully submitted,

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APPLICATION INFORMATION

Title Line One:: POWER SEMICONDUCTOR DIE ATTACH PROCESS U
Title Line Two:: SING CONDUCTIVE ADHESIVE FILM

Total Drawing Sheets:: 2
Formal Drawings?:: Yes
Application Type:: Utility
Docket Number:: IR17732-2498
Secrecy Order in Parent Appl.?:: No

CONTINUITY INFORMATION

This application is a:: NON PROV. OF PROVISIONAL
> Application One:: 60/167,456
Filing Date:: 11-24-1999

Source:: PrintEFS Version 1.0.1

Title: **POWER SEMICONDUCTOR DIE ATTACH PROCESS USING CONDUCTIVE ADHESIVE FILM**

Inventor(s): **MARK PAVIER**

RELATED APPLICATIONS

This application relates to and claims the filing date of United States Provisional Application Serial No. 60/167,456 (IR-1773 PROV (2-2141)), filed November 24, 1999.

BACKGROUND OF THE INVENTION

This invention relates to semiconductor devices and more specifically relates to a novel process for the attachment of power semiconductor die to a thermally and/or electrically conductive support.

Power semiconductor die such as diodes, MOSFETs, IGBTs and the like are normally attached to conductive lead frames or other substrates by electrically conducting materials such as epoxies, thermoplastics, solders and the like or by electrically insulative materials if electrical isolation is desired. This process is carried out sequentially for individual die, after die singulation from a wafer and is time consuming.

BRIEF DESCRIPTION OF THE INVENTION

In accordance with the invention adhesive films which may be electrically conductive or insulative are used as the die attach material for power semiconductors. Further, such adhesive films are attached to power semiconductor wafers before the die

singulation stage.

Adhesive films are now used to bond low power integrated circuits to lead frames. In accordance with the invention, electrically conductive or insulative adhesive films are used to bond power semiconductors to substrates/lead frames.

Adhesive films in the prior art are pre-cut and placed onto a substrate before the placement of die on the film. The resultant substrate/film/die assembly is then partially heat treated to promote adhesion between die/lead frame. In accordance with the invention, the adhesive film is placed onto the power semiconductor wafer before the die singulation stage. The wafer/adhesive film stack is then sawn using conventional singulation methods, producing die with the adhesive film pre-attached. The sawn die/film stack is then placed onto a substrate/lead frame before re-activating the adhesive via heat treatment to promote bonding and complete the curing.

There are a number of benefits provided by the invention. Thus, conventional power semiconductor die attach involves use of epoxy or solder type adhesives in paste or liquid form. These materials often overspill from the edge of the die onto the substrate/lead frame during die bonding. This overspill limits the size of die that can be placed on the lead frame/substrate. By using an adhesive film, such overspill is eliminated. Larger die can then be placed in a package of a given size. Bond line thickness is also set by the adhesive film thickness and will be constant. Voids in the bond will also be absent.

Pre-bonding electrically conductive or (electrically isolating) adhesive film onto the power semiconductor wafer before die singulation also removes the requirement of an extra pick and place stage during assembly. Manufacturing equipment costs and cycle times are therefore reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 and 2 are top and side views respectively of a prior art die attach.

Figure 3 and 4 are top and side views respectively of a power semiconductor die attached to a substrate by a conductive adhesive film.

Figure 5 is a perspective diagram of a large area adhesive film and a semiconductor device wafer before singulation.

Figure 6 is a perspective diagram of Figure 5 after adhesion.

Figure 7 shows one die/film stack singulated from the assembly of Figure 6 before attachment to a substrate.

Figure 8 shows the assembly of Figure 8 after heat cure and bonding.

Figure 9 shows the process of the invention as applied to a die-on-die assembly.

Figure 10 shows the process of the invention as applied to a side-by-side assembly of die on a common substrate.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

Figures 1 and 2 show a prior art power semiconductor die 10 and a conductive substrate 12 to which it is attached by a solder or epoxy attach material 11. Note that material 11 conventionally overspills, thereby limiting the maximum size of the die on a substrate of given area.

Figure 3 and 4 show the die 10 of Figures 1 and 2 where a thin, flexible adhesive film 13 is used to bond the die 10 and substrate 11. Film 13 is electrically conductive or may be insulative, and is heat curable. The use of such film is seen in Figures 3 and 4 to eliminate overspill, thus enabling a larger area die 10 on the substrate 11 of same area as that of Figures 1 and 2.

The novel process of the invention is shown in Figures 5 to 8. Figure 5 shows

a semiconductor device wafer 21 which contains a large number of identical power semiconductor die which are simultaneously processed in a conventional manner. Thus, the wafer can contain hundreds of identical vertical conduction power MOSFET die which have P/N junctions in their top surface, conventionally covered by a conductive source electrode and a bottom conductive drain electrode. The die of the wafer are singulated by sawing the wafer with conventional sawing apparatus. The individual die are then to be mounted on a lead frame or other substrate by soldering or epoxy bonding the drain electrode of the die to the substrate.

In accordance with the invention, an adhesive film 20 is cut to the size of the wafer, which can have a typical diameter of about 6 inches.

Film 20 is preferably a polyimide film such as that know as a "KAPTON" film which is frequently used in PC boards, "flex" circuits, for electrical winding insulation and the like. The Kapton polyimide is an excellent insulator. The wafer 21 and film 20 are then laid atop one another and are preheated to promote adhesion, but to not fully cure the film 20.

Thereafter, and as schematically shown in Figure 6 the film 20 and wafer 21 are simultaneously sawn at cut lines 22 into separate die. A conventional frame or support keeps the separated film/die stacks in place and the stacks are then placed into a conventional pick and place device so that the singulated devices can be picked up and carried to a location to be mounted on respective heated lead frames or substrates in an automated manner.

Thus, as shown in Figure 7 the die/film stack 21/20 can be picked up and placed atop a respective substrate 11 with a conventional pick and place apparatus. Pressure is preferably applied to press the stack 21/20 onto the surface of the pre-heated substrate 11.

Thereafter, the die/film stack 21/20 and substrate 11 are heated to about 260°C to fully heat cure film 21 to form a bond to the substrate 11.

The structure of figures 7 and 8 can also be carried out to form die-on-die

packages (Figure 9) or side-by-side die packages (Figure 10). Thus, in Figure 9, two identical die 30 and 31 or die with un-equal dimensions having adhesive layers 20 and semiconductor die 21 may be mounted with die 31 atop die 30. Die 30 and 31 may be diverse devices, for example, a MOSFET and a Schottky diode respectively and may be of different sizes or areas. Alternatively, die 31 can be an integrated circuit.

Further, layers 20 in Figure 9 can be a suitable electrically conductive adhesive film to allow back-to-back connection of die 30 and 31.

As shown in Figure 10, the die 30 and 31 may contain a MOSFET and an IC respectively (die 21).

Other film which can be used for film 20 includes thermoplastic adhesive paste such as Alpha Metals 383G (RHS) and UH2W-E polyimide film (LHS).

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. It is preferred, therefore, that the present invention be limited not by the specific disclosure herein, but only by the appended claims.

I CLAIM:

1. The process of connecting semiconductor die to a substrate:

said process comprising the steps of adhering a thin, flexible, heat curable film which is at least partially cured and is of a first area, to a thin semiconductor wafer of a second area and which contains a plurality of laterally displaced, identical semiconductor die of respective third areas which are each substantially less than the area of said first area;

thereafter simultaneously singulating both said heat curable film and said plurality of identical die to form individual elements each being of the area of said die and a matching area of adhesive film adhered to one surface of said die;

thereafter applying said singulated die to the top surface of said substrate surface with the film on said die pressed against said top surface; and

thereafter fully curing said film to firmly adhere said die to said substrate.

2. The process of Claim 1 wherein said substrate is a conductor lead frame.

3. The process of Claim 1 wherein said film is a polyimide.

4. The process of Claim 2 wherein said film is a polyimide.

5. The process of Claim 1 wherein said film on said die has the same or different area as that of said die after assembly onto said substrate.

6. The process of Claim 1 which includes the further step of adhering a

second semiconductor die with a second adhesive film thereon to said substrate at a position laterally removed from the first die.

7. The process of Claim 1 which includes the further step of adhering a second die with a second adhesive film thereon to the top of said die secured to said substrate.

8. The process of Claim 1 wherein said first area is substantially identical to, or different from, said second area.

9. The process of Claim 1 wherein said die and film are moved to said substrate by pick-and-place apparatus.

10. The process of Claim 1 wherein said adhesive film has a smaller area than said top surface of said die.

11. The process of Claim 7 wherein said adhesive film has a smaller area than said top surface of said die and wherein said second die and said second adhesive film both have the same area as said adhesive film.

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POWER SEMICONDUCTOR DIE ATTACH PROCESS USING ADHESIVE FILM

ABSTRACT OF THE DISCLOSURE

A large area adhesive film is attached to a semiconductor wafer containing a large number of identical structures. The film and wafer are then simultaneously singulated and the individual die with film thereon are then placed atop a lead frame and the film is completely cured to adhere the semiconductor die to the lead frame. Plural die can be mounted side-by-side on a common substrate, or one die can be mounted atop a second die which is on the substrate.

FIG. 1

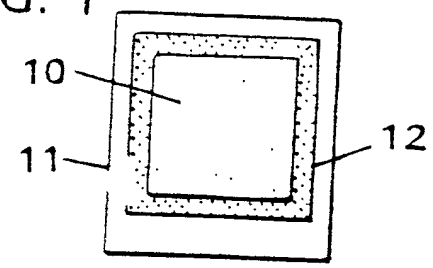


FIG. 3

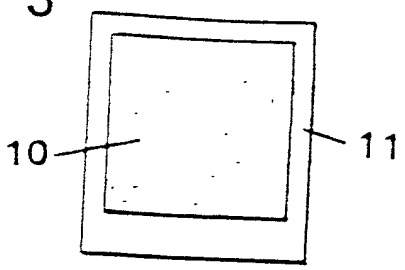


FIG. 2

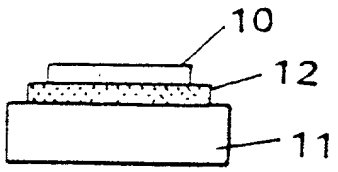
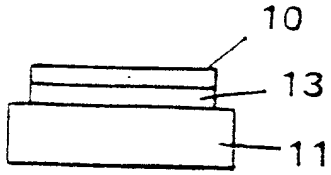


FIG. 4



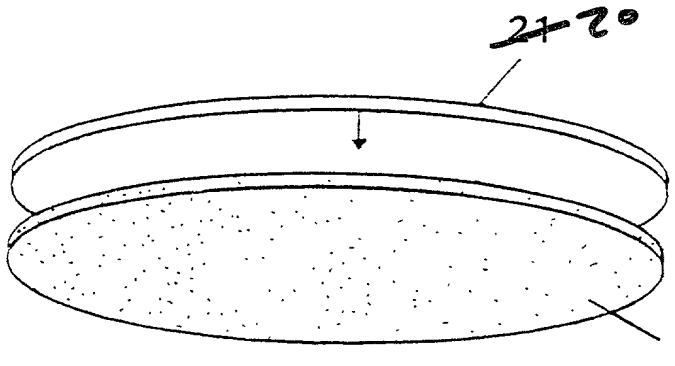


FIG. 5

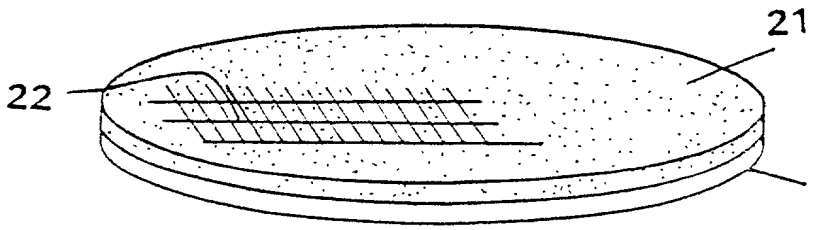


FIG. 6

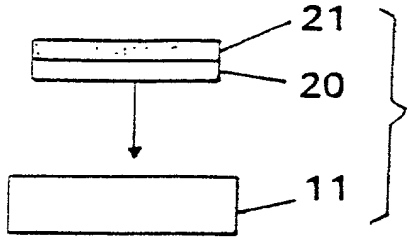


FIG. 7

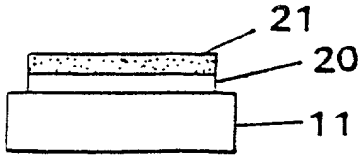


FIG. 8

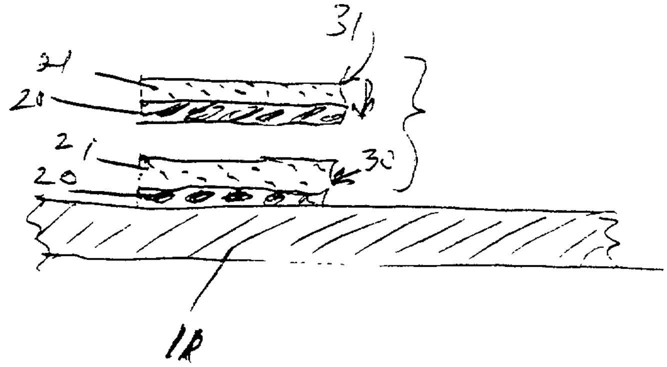


FIGURE 9

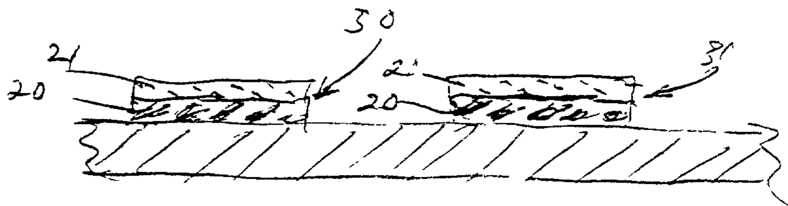


FIGURE 10

UNITED STATES OF AMERICA
COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

OFGS FILE NO.
IR-1773 (2-2498)

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

POWER SEMICONDUCTOR DIE ATTACH PROCESS USING ADHESIVE FILM

the specification of which is attached hereto, unless the following box is checked:

☐ was filed on _____ as United States patent Application Number or PCT International patent application number _____ and was amended on _____ (if any).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim priority benefits under Title 35, United States Code §119 of any foreign application(s) for patent or inventor's certificate or United States provisional application(s) listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign or Provisional Application(s)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. 119
United States	**60/167,456**	**24 November 1999**	YES _X_ NO ___
			YES ___ NO ___
			YES ___ NO ___

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

UNITED STATES APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby appoint customer no. 2352 OSTROLENK, FABER, GERB & SOFFEN, LLP, and the members of the firm, Samuel H. Weiner - Reg. No. 18,510; Jerome M. Berliner - Reg. No. 18,653; Robert C. Faber - Reg. No. 24,322; Edward A. Meilman - Reg. No. 24,735; Stanley H. Lieberstein - Reg. No. 22,100; Steven I. Weisburd - Reg. No. 27,409; Max Moskowitz - Reg. No. 30,576; Stephen A. Soffen - Reg. No. 31,063; James A. Finder - Reg. No. 30,173; William C. Gray, III - Reg. No. 30,944; Louis C. Dujmich - Reg. No. 30,625 and Douglas A. Miro - Reg. No. 31,643, as attorneys with full power of substitution and revocation to prosecute this application, to transact all business in the Patent & Trademark Office connected therewith and to receive all correspondence.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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RESIDENCE (City and either State or Foreign Country)		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		